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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,004	08/17/2004	Kent Kuohua Chang	9946-US-PA-1	5003

31561 7590 05/16/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
GUERRERO, MARIA F	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,004	CHANG, KENT KUOHUA	
	Examiner	Art Unit	
	Maria Guerrero	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is the First Office Action on the merits.

Status of Claims

2. Claims 1-5 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 5 recites the tunneling dielectric layer is formed with a material selected from the group consisting of ZrO2, HfO2 and ZrOxNy; the independent claim 1 recites the tunneling dielectric layer is formed with a material selected from the group **consisting of** HfSiON and HfOxNy.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimoji (US 5,349,221) in view of Shanware et al. "Reliability evaluation of HfSiON gate dielectric film with 12.8 a SiO2 equivalent thickness".

Shimoji teaches a memory device comprising: a substrate (11), a tunneling dielectric layer (16) disposed over the substrate (11), an electron trapping layer (17) disposed over the tunneling dielectric layer (16), a top oxide layer (18) disposed over the electron trapping layer (17) (Fig. 1, col. 4, lines 35-60). Shimoji shows the tunneling dielectric layer, the electron trapping layer, and the top oxide layer forming a stacked structure (Fig. 1). Shimoji discloses a conductive layer (20) disposed over the top oxide layer (18), a drain region in the substrate beside both sides of the stacked structure (Fig. 1, col. 4, lines 35-60).

Shimoji does not specifically show the tunneling dielectric layer being formed from HfSiON. However, Shanware et al. suggested replacing the conventional silicon oxide by HfSiON in order to reduce gate-leakage and improve reliability (pages 137-140).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Shimoji reference by including the HfSiON instead of silicon oxide in order to reduce gate-leakage and improve reliability of the device (Shanware et al., abstract).

5. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US 6,468,865) in view of Shanware et al. "Reliability evaluation of HfSiON gate dielectric film with 12.8 a SiO2 equivalent thickness".

Yang et al. teaches a memory device comprising: a substrate (12), a tunneling dielectric layer disposed over the substrate (14a), an electron trapping layer disposed

over the tunneling dielectric layer (14b), a top oxide layer disposed (14c) over the electron trapping layer (14b) (col. 5, lines 40-50). Yang et al. shows the tunneling dielectric layer, the electron trapping layer, and the top oxide layer forming a stacked structure (Figs. 8,16). Yang et al. discloses a conductive layer (28) disposed over the top oxide layer (14c), a drain region and an oxide layer disposed over the drain region in the substrate beside both sides of the stacked structure (Figs. 8,15-16, col. 9, lines 30-35, col. 12, lines18-35).

Yang et al. does not specifically show the tunneling dielectric layer being formed from HfSiON. However, Shanware et al. suggested replacing the conventional silicon oxide by HfSiON in order to reduce gate-leakage and improve reliability (pages 137-140).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Yang et al. reference by including the HfSiON instead of silicon oxide in order to reduce gate-leakage and improve reliability of the device (Shanware et al., abstract).

6. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US 6,468,865) in view of Kang et al. "Improved Thermal Stability and device performance of ultra-thin (EOT<10A) gate dielectric MOSFETs by using hafnium oxynitride (HfOxNy)".

Yang et al. teaches a memory device comprising: a substrate (12), a tunneling dielectric layer disposed over the substrate (14a), an electron trapping layer disposed

over the tunneling dielectric layer (14b), a top oxide layer disposed (14c) over the electron trapping layer (14b) (col. 5, lines 40-50). Yang et al. shows the tunneling dielectric layer, the electron trapping layer, and the top oxide layer forming a stacked structure (Figs. 8,16). Yang et al. discloses a conductive layer (28) disposed over the top oxide layer (14c), a drain region and an oxide layer disposed over the drain region in the substrate beside both sides of the stacked structure (Figs. 8,15-16, col. 9, lines 30-35, col. 12, lines18-35).

7. Yang et al. does not specifically show the tunneling dielectric layer being formed from HfOxNy. However, Kang et al. suggested improving thermal stability and device performance by using HfOxNy as gate dielectric material. Kang et al. also shows the use of HfO2 and ZrOxNy as conventional in the art (pages 146-147).

8. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify Yang et al. reference by including the HfOxNy suggested by Kang et al. in order to improve thermal stability and device performance (Kang et al., page 146).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Laaksonen et al. “Advanced CMOS transistors with a novel HfSiON gate dielectric” and Rotondaro et al. “Carrier mobility in MOSFETs fabricated with Hf-Si-O-N gate dielectric, polysilicon gate electrode, and self-aligned source and drain” describe the use of HfSiON as a gate dielectric.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Maria Guerrero whose telephone number is 571-272-1837.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 11, 2005

maría Guerrero

MARIA F. GUERRERO
PRIMARY EXAMINER